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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,138	10/17/2003	Thomas P. Glenn	AMKOR-025C1	2017

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EXAMINER	
OWENS, DOUGLAS W	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,138	GLENN ET AL.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *41-43 and 46* is/are allowed.

6)☒ Claim(s) *31-36,38-40 and 48-50* is/are rejected.

7)☒ Claim(s) *37,44,45 and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 31 – 36, 38 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,198,171 to Huang et al.

Regarding claim 31, Huang et al. teach a semiconductor package (Figs. 3 and 4, for example) comprising:

a die pad (200) having opposed, generally planar first and second surfaces, and peripheral side surfaces which extend between the first and second surfaces;

a plurality of leads (202) extending about the die pad in spaced relation to the side surfaces thereof, each of the leads having:

opposed, generally planar first (206b) and second (206a) surfaces;

peripheral side surfaces extending between the first and second surfaces;

an inner lead portion defining an inner end surface; and

an outer lead portion, a portion of the first surface (206b) defined by the outer lead portion being sized and configured for electrical connection to a conductive terminal;

a semiconductor chip (208) attached to the first surface of the die pad and electrically connected to at least one of the leads; and

a package body (218) at least partially encapsulating the semiconductor chip, the die pad, and the leads such that the inner lead portion of each of the leads is within the package body and the outer lead portion of each of the leads extends out of the package body.

Regarding claim 32, Huang et al. teach a semiconductor package, wherein the inner end surface of each of the leads and portions of the first and side surfaces of each of the leads which extend along the inner lead portion thereof are covered by the package body.

Regarding claim 33, Huang et al. teach a semiconductor package, wherein the package body has opposed, generally planar first and second surfaces and a portion of the second surface of each of the leads which extends along the inner lead portion thereof is exposed in and substantially flush with the second surface of the package body.

Regarding claim 34, Huang et al. teach a semiconductor package, wherein the first and side surfaces of the die pad are covered by the package body.

Regarding claim 35, Huang et al. teach a semiconductor package, wherein the second surface of the die pad is exposed in and substantially flush with the second surface of the package body.

Regarding claim 36, Huang et al. teach a semiconductor package, wherein the semiconductor chip is electrically connected to the first surface of at least one of the leads via a conductive wire (216) which is encapsulated by the package body.

Regarding claim 38, Huang et al. teach a semiconductor package, wherein each of the leads includes and undercut region, which is disposed in the second surface thereof, and the package body covers the undercut region.

Regarding claim 40, Huang et al. teach a semiconductor package (Fig. 7), further in combination with a second semiconductor chip (310) attached to the semiconductor chip and electrically connected to at least one of the leads, the second semiconductor chip being covered by the package body.

3. Claims 31, 38 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,420,779 to Sharma et al.

Regarding claim 31, Sharma et al. teach a semiconductor package (Fig. 1, for example) comprising:

a die pad (120) having opposed, generally planar first and second surfaces, and peripheral side surfaces which extend between the first and second surfaces;

a plurality of leads (130,140) extending about the die pad in spaced relation to the side surfaces thereof, each of the leads having:

opposed, generally planar first (132) and second (131) surfaces;

peripheral side surfaces extending between the first and second surfaces;

an inner lead portion defining an inner end surface; and

an outer lead portion, a portion of the first surface defined by the outer lead portion being sized and configured for electrical connection to a conductive terminal;

a semiconductor chip (110) attached to the first surface of the die pad and electrically connected to at least one of the leads; and

a package body (150) at least partially encapsulating the semiconductor chip, the die pad, and the leads such that the inner lead portion of each of the leads is within the package body and the outer lead portion of each of the leads extends out of the package body.

Regarding claim 38, Sharma et al. teach a semiconductor package, wherein each of the leads includes and undercut region, which is disposed in the second surface thereof, and the package body covers the undercut region.

Regarding claim 39, Sharma et al. teach a semiconductor package, wherein the die pad includes an undercut region which is disposed in the second surface thereof and extends to the side surfaces thereof and the undercut region is covered by the package body.

4. Claims 48 – 50 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,756,380 to Berg et al.

Regarding claim 48, Berg et al. teach a semiconductor package (Fig. 2, for example), comprising:

a substrate (110) having opposed first and second surfaces;

a die pad (116; Col. 10, lines 10 – 14) disposed on the first surface of the substrate;

a plurality of circuit patterns (112) disposed on the first surface of the substrate and extending at least partially about the die pad in spaced relation thereto, each of the circuit patterns having an inner end portion and an outer end portion;

a semiconductor chip (102) attached to the die pad and electrically connected to at least one of the circuit patterns; and

a package body (130) at least partially encapsulating the semiconductor chip, the substrate and the circuit patterns such that the inner end portion of each of the circuit patterns is covered by the package body and the outer end portion of each of the circuit patterns is exposed outside of the package body to serve as an input/output terminal.

Regarding claim 49, Berg et al. teach a semiconductor package, wherein the substrate includes a plurality of input/output terminals (132) which are disposed on the second surface thereof and electrically connected to respective ones of the circuit patterns.

Regarding claim 50, Berg et al. teach a semiconductor package, wherein the semiconductor chip is electrically connected to the inner end portion of at least one of the circuit patterns via a conductive wire (124), which is encapsulated by the package body.

Response to Arguments

5. Applicant's arguments filed January 10, 2005 have been fully considered but they are not persuasive.

Applicant argues that Huang et al. do not teach a device, wherein a first surface of the outer lead portion is sized and configured for electrical connection to a conductive terminal. This feature is shown in figure 3 of Huang et al., where the first surface (206b) is sized and configured for electrical connection to a conductive terminal. Huang further discloses that the first surface (206b) is exposed for the purpose of external connection (Col. 4, lines 14 – 18).

Applicant argues that Sharma et al. do not teach a device, wherein a first surface of the outer lead portion is sized and configured for electrical connection to a conductive terminal. This feature is shown in figure 1 of Sharma et al., where the first surface (132) is sized and configured for electrical connection to a conductive terminal. Sharma et al. further disclose that the first surface (132) is exposed for electrical connection to a PCB (Col. 4, lines 1 – 4).

Applicant argues that Berg et al. do not teach a device including circuit patterns that extend outside of the package body and serve as input/output terminals. This teaching can be seen in figure 2, where the circuit patterns (112) extend outside of the package body (130), electrically connecting the chip to solder balls (132). Accordingly, the circuit patterns serve as input/output terminals since they provide communication means inside and out of the packaged device.

Allowable Subject Matter

6. Claims 41 – 43 and 46 are allowed.

7. Claims 37 and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DWO

EDDIE LEE
SPE TC 2800